CLAIMS

1. A method for programming at least one portion of a memory cell with a first programmed value, the method comprising:

injecting charge having a first polarity into a first plurality of discrete charge storage elements within the memory cell;

injecting charge having a second polarity into a portion of the first plurality of discrete charge storage elements; and

using the first plurality of discrete charge storage elements to represent the first programmed value.

2. A method as in claim 1, wherein the charge having the first polarity is injected by electrons and wherein the charge having the second polarity is injected by holes.

3. A method as in claim 1, further comprising:

before said step of injecting charge having a first polarity, determining if a present logic state of the at least one portion of the memory cell is different than the first programmed value.

4. A method as in claim 1, wherein the first programmed value is one of a logic state one and a logic state zero.

5. A method as in claim 1, further comprising providing a plurality of memory cells in a memory that is a non-volatile memory.

6. A method as in claim 5, further comprising implementing the memory as an electrically erasable programmable memory.

7. A method as in claim 1, wherein the memory cell has a first portion and a second portion, and wherein the first plurality of discrete charge storage elements are located in the first portion of the memory cell.

8. A method as in claim 7, further comprising:

determining if a present logic state of the first portion of the memory cell is different than the first programmed value;

if the present logic state of the first portion of the memory cell is different than the first programmed value, performing said step of injecting charge having a first polarity;

determining if a second programmed value to be programmed into the second portion of the memory cell is different than the first programmed value; and

if the second programmed value is different than the first programmed value, performing said step of injecting charge having a second polarity.

9. A method as in claim 7, further comprising:

injecting charge having a first polarity into a second plurality of discrete charge storage elements within the second portion of the memory cell;

injecting charge having a second polarity into a portion of the second plurality of discrete charge storage elements; and

using the second plurality of discrete charge storage elements to represent a second programmed value.

10. A method as in claim 1, further comprising:

providing the memory cell in an erased state before said step of injecting charge having a first polarity.

11. A memory, comprising:

means for injecting charge having a first polarity into a first plurality of discrete charge storage elements within a portion of the memory;

means for injecting charge having a second polarity into a portion of the first plurality of discrete charge storage elements; and

means for retrieving a programmed value from the first plurality of discrete charge storage elements.

12. A memory as in claim 11, wherein the means for injecting charge having the second polarity can concurrently inject charge to a plurality of memory cells within a row of the memory.

13. A memory as in claim 11, wherein the means for injecting charge having the second polarity can concurrently inject charge to a plurality of memory cells within a column of the memory.

14. A memory, comprising:

a memory cell having a first portion and a second portion, said first portion having a first state and said second portion having a second state;

a sense amplifier coupled to said memory cell wherein said sense amplifier senses the first state of said first portion and second state of said second portion; and

program circuitry coupled to said sense amplifier, whereby based on a comparison of the first state and second state, charge is selectively injected into at least one of said first portion and said second portion.

15. A memory as in claim 14, wherein said charge is selectively injected during programming of at least one portion of the memory cell.

16. A memory as in claim 14, wherein said charge comprises holes which are selectively injected during programming of at least one portion of the memory cell.

17. A memory as in claim 16, wherein said memory cell is located within a row of memory cells, and wherein said charge is injected into a plurality of memory cells within the row based on logic states stored in the plurality of memory cells.

18. A memory as in claim 14, wherein said charge is selectively injected when the first state and said second state are of opposite states.

19. A memory as in claim 14, wherein said charge comprises electrons.

20. A memory as in claim 14, wherein the memory is a non-volatile memory.

21. A memory as in claim 14, wherein the memory is an electrically erasable programmable memory.